IN THE CLAIMS

Please amend the claims as follows.

Claim 1 (cancelled)

Claim 2 (currently amended): ~~The frequency synthesizing circuit according to claim 1, wherein~~ A frequency synthesizing circuit comprising a frequency multiplier and a phase-locked loop, wherein an external reference signal which is frequency doubled by said frequency multiplier is employed to be a reference signal of said phase-locked loop for increasing the loop bandwidth of said phase-locked loop said frequency multiplying circuit comprises a delay phase-locked loop and a phase synthesizer, said delay phase-locked loop is utilized to generate multiphase outputs which equivalently divide a cycle of said reference signal, and said phase synthesizer utilizes said multiphase output to synthesize an equivalent frequency multiplying signal.

Claim 3 (original) A frequency synthesizing circuit comprising a multiphase generator, a multiplexer, a phase selector and a phase-locked loop, wherein frequency multiplication is achieved by synthesizing different output phases generated from said multiphase generator whose phases are selected outputted to the phase synthesizer by said multiplexer incorporated with a phase selector and the output of said phase synthesizer is employed to be a reference signal of said phase-locked loop.

Claim 4 (original) The frequency synthesizing circuit according to claim 3, wherein said multiphase generator comprises a delay phase-locked loop which generate said multiphase outputs that equivalently divide a cycle of said reference signal and is cooperated with said phase selector and said multiplexer to be outputted to said

phase synthesizer so as to synthesize different frequency multiplying signals through said phase synthesizer.